UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/885,426	06/19/2001	Daniel Sobek	AMD-E306	4225

7590 03/25/2005

Wagner Murabito & Hao LLP
Two North Market Street
Third Floor
San Jose, CA 95113

EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/885,426	SOBEK ET AL.	
	Examiner	Art Unit	
	Quang D. Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 15, 16-18, 21, 22 and 26-30 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,879,990 to Dormans et al.

Regarding claim 15, Dormans et al. (figures 1-8) teach forming an oxide (6) over the bitlines (24, 25).

Regarding claim 16, Dormans et al. (figures 1-8) teach a process of fabricating a memory cell comprising a substrate that comprises a first region and a second region with a channel therebetween, the method comprising:

forming a gate (22) above the channel (a region is formed under gate [22]) of the substrate (1), wherein the gate (22) comprises a single polysilicon layer (column 3, lines 65-67);

forming bitlines (24, 25) on both sides of the gate (22) subsequent to the forming the gate (22); and

siliciding (26) the bitlines (24, 25).

Regarding claim 17, Dormans et al. teach siliciding (26) the single polysilicon layer (22).

Regarding claim 18, Dormans et al. teach the siliciding (26) of the bitlines (24, 25) and the single polysilicon layer (22) occur simultaneously.

Regarding claim 21, Dormans et al. teach the gate layer (22) comprises an N-type material (column 3, lines 65-67).

Regarding claim 22, Dormans et al. teach the gate (22) comprises a polycrystalline silicon (column 3, lines 65-66).

Regarding claim 26, Dormans et al. teach the memory cell comprises an EEPROM memory cell (column 1, lines 33-36).

Regarding claim 27, Dormans et al. inherently teach the memory cell comprises a two-bit memory cell because it enhances the density of data on the same chip area without increasing size of the memory cell.

Regarding claim 28, Dormans et al. teach the substrate (1) a p-type substrate (column 3, lines 46-47).

Regarding claim 29, Dormans et al. inherently teach scaling the length of the bitlines for fitting the bitlines into the device.

Regarding claim 30, note that the scaling comprises reducing the thermal cycle of the bitlines is a functional language and does not further limit or define the structure and is not given any patentable weight. Additionally, the device taught by Dormans et al. could have been used for the claimed purpose.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 19-20 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,879,990 to Dormans et al. in view of US Patent No. 6,218,695 to Nachumovsky.

Regarding claim 19, Dormans et al. differ from the claimed invention by not showing forming a charge-trapping region that contains a first amount of charge. However, Nachumovsky (figure 1) teaches forming a charge-trapping region that contains a first amount of charge (electron jump into the nitride layer [20] by hot electron injection; column 1, lines 25-30). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Nachumovsky into the device taught by Dormans et al. in order to store the electron in the nitride layer.

The combined device shows forming a layer (Nachumovsky; 18) between the channel (Nachumovsky; 17) and the charge-trapping region (Nachumovsky; 20). It is inherent that the layer has a thickness such that the first amount of charge is prevented from directly tunneling into the layer because the first amount of charge (electron) jumps into the charge storage region by hot electron injection.

Regarding claim 20, the combined device shows the charge trapping region (Nachumovsky; 20) comprises silicon nitride.

Regarding claim 23, the combined device shows forming an insulating layer (Nachumovsky; 22) on the charge-trapping region (Nachumovsky; 20).

Regarding claim 24, the combined device shows the insulating layer (Nachumovsky; 22) comprises silicon dioxide.

Regarding claim 25, the combined device shows the charge trapping region (Nachumovsky; 18) comprises silicon dioxide.

Response to Arguments

Applicant's arguments with respect to claims 15-30 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D. Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv

EDDIE LEE
SPE TC 2800